In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1-18. Canceled.

19. (original) An integrated circuit produced from a photolithographic mask of a target pattern in a layer of material of the integrated circuit, the layer of material of the integrated circuit comprising:

a plurality of features defined by a plurality of shifter shapes of the photolithographic mask within a maximum shifter area around the plurality of features in the target pattern, such that the shifter shapes run along edges of the plurality of features, the plurality of shifter shapes having phases assigned according to phase dependencies and costs, the plurality of shifter shapes having one or more refinements filling at least part of space originally left between adjacent shifter shapes to admit a cut.

20. (original) The integrated circuit of claim 19, wherein at least one feature of the plurality of features was defined by a complementary photolithographic mask from the target pattern and the plurality of shifter shapes.

21. (original) The integrated circuit of claim 19, wherein the phases are computed according to costs corresponding to a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

22. (original) The integrated circuit of claim 19, wherein the phases are assigned via branch-and-bound.

23. (original) The integrated circuit of claim 19, wherein the maximum shifter area includes one or more end-caps of at least one feature of the plurality of features.

24. (original) The integrated circuit of claim 23, wherein the maximum shifter area accounts for endcap cutting protection.

25. (original) The integrated circuit of claim 19, wherein the maximum shifter area is defined by spatially padding the plurality of features with a distance and drawing a border around the plurality of features so that the border is spaced away from the plurality of features by the distance.

26. (original) The integrated circuit of claim 25, wherein the border of the maximum shifter area runs closer than the distance to features of the plurality of features having at least one endcap.

27. (original) A method of manufacturing an integrated circuit having a layer of material described by a layout, the method comprising:

identifying a plurality of features in the layout to be defined using phase shifting;

exposing radiation sensitive material to radiation according to the target pattern defined using a plurality of shifter shapes of a photolithographic mask within a maximum shifter area around a plurality of features in the target pattern, such that the shifter shapes run along edges of the plurality of features, the plurality of shifter shapes having phases assigned according to phase dependencies and costs, the plurality of shifter shapes having one or more refinements filling at least part of space originally left between adjacent shifter shapes to admit a cut; and

developing the exposed radiation sensitive material to define the layout, and forming said layer of material according to the layout.

28. (original) The method of claim 27, wherein at least one feature of the plurality of features was defined by a complementary photolithographic mask from the layout and the plurality of shifter shapes.

29. (original) The method of claim 27, wherein the phases are computed according to costs corresponding to a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner

corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

30. (original) The method of claim 27, wherein the phases are assigned via branch-and-bound.

31. (original) The method of claim 27, wherein the maximum shifter area includes one or more end-caps of at least one feature of the plurality of features.

32. (original) The method of claim 31, wherein the maximum shifter area accounts for endcap cutting protection.

33. (original) The method of claim 27, wherein the maximum shifter area is defined by spatially padding the plurality of features with a distance and drawing a border around the plurality of features so that the border is spaced away from the plurality of features by the distance.

34. (original) The method of claim 33, wherein the border of the maximum shifter area runs closer than the distance to features of the plurality of features having at least one endcap.
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